DETAILED ACTION

This office action is in response to the applicant's amendment dated 4/14/2008.

The applicant has cancelled claims 21, 23 and 25.

The applicant has amended claims 2, 4, 16, 18-20, 22, 24 and 26.

Claims 2-7, 9-14, 16-20, 22, 24 and 26 are pending.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with David Raczkowski on 5/6/2008.

The application has been amended as follows:

Claim 22: Line 9 of the claim is amended to recite;

inputting the set of test data into the reconfigurable device to create a set of test results;

Claim 26: The claim is amended as follows;

Claim 26. (Currently Amended by examiner) A reconfigurable device comprising an information storage medium including a test configuration for configuring the reconfigurable device, the reconfigurable device having an IP core implementing at least one specialized operation and a set of functional blocks adapted to implement general-purpose logic devices, the test configuration comprising a configuration of

the set of functional blocks implementing a set of boundary scan registers connected with a set of interface connections of the IP core,

~~wherein when the reconfigurable device is configured in the test configuration, the set of functional blocks are configured to implement the set of boundary scan registers, the set of boundary scan registers including at least one input register, the input register having an input coupled to an output of a multiplexer and an output coupled to a first input of a logic gate, where a select input for the multiplexer is coupled to a second input of the logic gate and an output of the logic Rate is coupled to an input of the IP core,~~

wherein when the reconfigurable device is configured in the test configuration, the set of functional blocks are configured to implement the set of boundary scan registers, the set of boundary scan registers including at least one input register, the input register having an input coupled to an output of a multiplexer and an output coupled to a first input of a logic gate, where a select input for the multiplexer is coupled to a second input of the logic gate and an output of the logic gate is coupled to an input of the IP core, wherein the output of the logic gate provides an output signal to an input of the multiplexer, and wherein the output of the input register provides a signal to an input of another input register in the set of boundary scan registers.

Response to Amendment

2. In view of the amendments to the claims including cancelling of claims 21, 23 and 25, the Examiner's Amendment above, the applicant's arguments in the Remarks of the amendment dated 4/14/2008 are persuasive, and so all objections and rejections to the claims and drawings previously outlined in the prior office action are withdrawn.

Allowable Subject Matter

3. Claims 2-7, 9-14, 16-20, 22, 24 and 26 are allowed. The following is an examiner's statement of reasons for allowance: As per independent claims 22, 24 and 26, the references of Herron, Jin, Kiryu and Suzumura have disclosed a method and software based on a reconfigurable device that comprises storage for a test configuration, an IP core, reconfigurable functional blocks, the blocks implementing a boundary scan chain that performs testing operations via an interface with the IP core, where a scan register is configured with a latch, a multiplexer, the latch output separately passing a scan signal to a next scan register input, and a logic gate to pass input data to the IP core. But the references have failed to further provide disclosure, or suggest the unique feature that is claimed by the applicant, wherein the logic gate output provides an input signal to the multiplexer. Consequently the independent claims 22, 24 and 26 are allowed, and in view of their dependence, claims 2-7, 9-14 and 16-20 are also allowed. The claims are to be renumbered as claims 1-20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN P. TRIMMINGS whose telephone number is (571)272-3830. The examiner can normally be reached on Monday through Thursday, 7:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John P Trimmings/
Primary Examiner,
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jpt